A Remote Line Concentrator for a Time-Separation Switching Experiment

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Remote line concentration, time-separation switching and PCM transmission are combined in a communication system experiment called ESSEX (Experimental Solid State Exchange). Organization and design details of the remote line concentrator used in the research model are presented and discussed.

I. INTRODUCTION

An earlier paper[1] has described a research experiment on integrated communications using time-separation techniques. This experiment is called ESSEX (Experimental Solid State Exchange). The purpose of this paper is to discuss the environment and implementation of the remote line concentrators used in the experiment.

ESSEX is an experiment designed to explore the possibilities of using digital systems in exchange area plant. Subscribers are connected to remote units that multiplex and convert analog signals to digital signals. Digital signals are transmitted and switched between remote units and are converted to analog form only at the units to which they are directed. The assemblages that provide the necessary switching and transmission functions for subscribers' lines are called *concentrators*; those that provide the switching and transmission functions for trunks are called *trunkors*. Concentrators and trunkors form the basic building blocks of the system.

A concentrator consists of two units called the *remote line concentrator* and the *concentrator controller*. The trunkor also has two parts, the *trunkor unit* and the *trunkor controller*. Since trunk groups ordinarily have high usage, the trunkor has no concentration, but otherwise it is identical to a concentrator.

The remote line concentrator can serve a maximum of 255 subscribers. In a working system, however, traffic considerations would probably

limit the number of subscribers to about 115, of whom 23 can converse simultaneously. Their voice-frequency signals are selectively switched by time-separation techniques and converted to digital form for transmission. Since digital signals are both sent and received by remote line concentrators, four-wire transmission is employed between them. Exchange cable pairs can be used for this purpose, with regenerative repeaters spaced every 6000 feet or less depending on the kind of cable.

The interconnection of the digital send and receive links from the remote units is made at a unit called the *central stage switch*, which uses four-wire switching on a time- and space-division basis. Time and space division are used to provide the necessary number of paths required when many concentrators are connected to the switch. The send and receive links from each unit are equipped with a time-division switch for each space-division link or *junctor* in the central stage switch. This provides a full-access space-division interconnection between junctors.

In setting up or maintaining a communication channel in ESSEX, the selective switch at the remote unit and the switch at the central stage switch are operated periodically, as is required in time-division systems. Memory is, therefore, required to deliver proper information at the right time to the switches. Several options on the location of the memory were considered, with the one option chosen being to locate all the memory close to the central stage switch. Another digital control pair, called the c lead, was therefore required to deliver address information to the remote unit. The remote unit thus becomes a completely slave-operated unit containing a minimum of equipment.

The memory required by the concentrator is contained in a unit called the *concentrator controller*. In addition to the line number and junctor gate number memory already referred to, this unit contains a third memory to record the state of the call being handled by the concentrator. These three memories are implemented with magnetostrictive delay lines, each arranged in a closed loop. The information in the delay line circulates in serial form and is available for transmission over the c lead to the remote line concentrator.

In addition to the memories, the concentrator controller contains circuits for checking and processing calls, as well as circuits that enable it to deliver and accept information from a common control. A complete description of all the functions performed by the concentrator controller is given in the accompanying paper.[2]

A typical arrangement of concentrators and trunkors is shown in Fig. 1. Here, the remote line concentrators are located some distance from a switching center, which contains the central stage switching, the con-

centrator controllers, the trunkor and possibly the common control. Since the bounds of the ESSEX experiment did not include an experimental investigation of common control, Fig. 1 shows, in its place, a manual console. This manual console, called the *common control simulator*, allows an operator to perform the logic and memory functions normally performed by a common control.

II. TRANSMISSION AND SWITCHING IN ESSEX

A clearer picture of some of the functional requirements of the remote line concentrator can be obtained by following a call through the system shown in Fig. 1. It will, however, be profitable to digress for a moment to give some of the important system numbers and define terms that will be used here and in the detailed discussion that follows.

Voice-frequency signals appearing on a subscriber's line are sampled at an 8000-cycle rate. This allows signal components up to 4000 cps to be reproduced by the low-pass filters in the remote line concentrators. When the signals are sampled at this rate, the period between samples

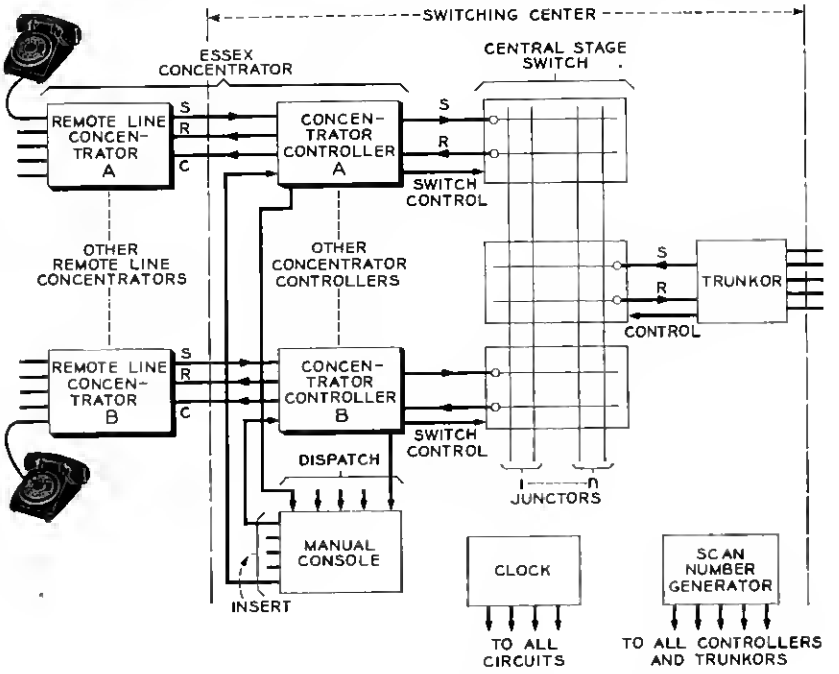

Fig. 1 — The environment of the remote line concentrator.

of the same message is 125 microseconds and is called a *frame*. Frames are subdivided into equal parts, called *time slots*, each of which can be used to set up a path to each concentrator. ESSEX uses 24 time slots, 23 being used for talking and one for supervisory functions. The time slots are numbered 0 to 23 and are each 5.2 microseconds long. This 5.2-microsecond interval is divided into eight pulse or bit positions, each 0.65 microsecond wide, numbered 0 through 7. On the R and S leads, bits 0 through 6 are used for pulse code modulation information (PCM) and bit 7 is used for other functions. The basic bit rate is thus 1.536 mc.

Returning now to Fig. 1, we can see that a voice-frequency signal appearing on a subscriber's line at remote line concentrator A is switched by an address arriving at remote line concentrator A via the C lead. The pulse-amplitude modulated (PAM) sample that results from the switching is then encoded and transmitted over a balanced cable pair, designated S, to concentrator controller A. From here it passes, still in digital form, to the central stage switch, where it is switched onto a cable pair, designated R, to concentrator B. Signals coming from the S lead of concentrator B are switched to the R lead of concentrator A. The junctor gates of concentrators A and B operate at the same time, which means that the same time slot is used in both concentrators in setting up a channel.

Since the junctor gates operate once per frame for each conversation, PCM signals from a concentrator must arrive at the central stage switch in phase with the PCM signals being sent to the concentrator. Remote line concentrators will, in general, be located at different distances from the switching centers, and their loop transmission delays will vary accordingly. If the loop transmission delay is one frame or an integral multiple of frames, this phase requirement will be met. This condition also can be achieved and maintained continuously by the insertion in the S lead of an adjustable delay pad, which is part of the concentrator controller. A more detailed description of the transmission delays is given in the companion papers.[1,2]

From a switching viewpoint, ESSEX uses a four-stage switching plan. Two of these stages are in the central stage switch; the other two are in the concentrators handling the call.

III. THE REMOTE LINE CONCENTRATOR

A block diagram of the remote line concentrator is shown in Fig. 2. The blocks represent multifunctional circuits that handle either analog or digital signals. The elements in the analog class are the subscriber line circuits, the two-to-four-wire converter, the compressor and the ex-

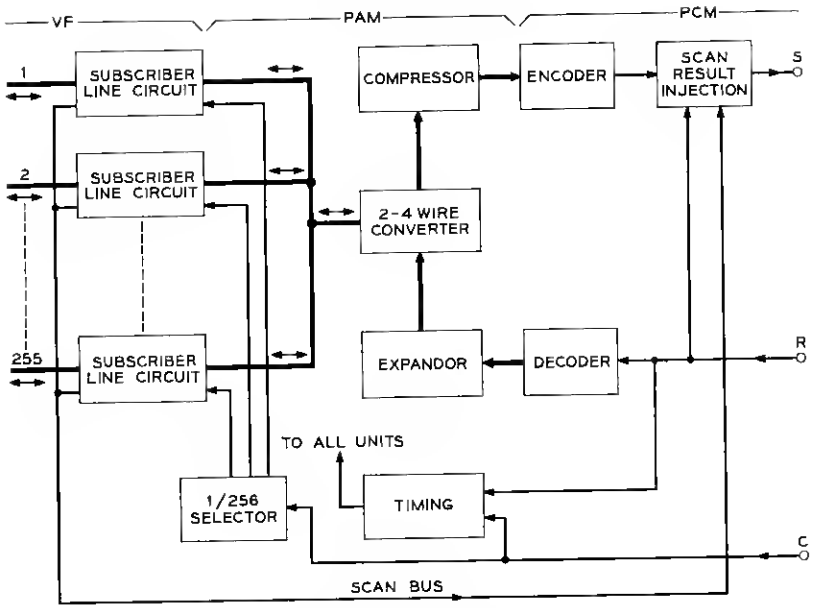

Fig. 2 — Block diagram of the remote line concentrator.

pandor. The remainder, which includes the encoder, the decoder, the selector, the line scan injection and the timing circuits, are digital. The purpose of each of these multifunctional circuits can be made clear by describing the operation of the remote line concentrator itself.

When an eight-bit address is delivered to the 1-out-of-256 selector via the C lead, the selector delivers a pulse to the subscriber's time-division gate. This gate, which is a part of the subscriber's equipment, samples the voice-frequency signal and delivers the resulting PAM signal to the two-to-four-wire converter, which is a time-shared hybrid. The PAM signal is sent through an instantaneous compressor to the encoder, and the resulting PCM code is delivered to the S lead. Signals arriving on the R lead are decoded, expanded, amplified in a common amplifier and sent through the time-shared hybrid to the subscriber's equipment.

Since the remote line concentrator is a slave unit, timing information must be recovered from the signals coming from the concentrator controller. Frequency information is extracted from signals arriving on the C lead, and phase information is obtained from a unique signal that appears on the R lead of each concentrator in the last time slot of each frame (time slot 23).

Line scanning for request-for-service and hang-up is a relatively simple procedure in ESSEX. A *scan number generator*, common to all

concentrator controllers, is provided. This device generates all the binary numbers from 0 to 255 and then repeats, with each number being generated and held for four frame intervals. A particular line gate number thus appears for four frames at the concentrator controller 7.8 times per second. If the line gate number that appears is already recorded in the line gate number memory of the concentrator controller, then the line is scanned in its assigned time slot. In this case, the *scan command*, which occurs at bit 7 time, is sent out on the R lead. If the line gate number is not in the memory, then it is scanned by sending out the line gate number over the C lead in time slot 23 during the first of the four frames. Four frames are used to allow time for the signals to be sent out to the remote line concentrator and return to the controller and for the controller to act on the result.

The lines at the remote line concentrator are scanned when the scan command appears on the R lead. The particular line number that is to be scanned is the one present at the input of the selector at this time. A scan gate is located in each subscriber's line circuit and, when a pulse is delivered from the 1-out-of-256 selector to the subscriber line circuit and the subscriber is "off-hook", the scan gate delivers a pulse to the scan bus. If the scan command is also present on the R lead, the scan flip-flop in the *scan result injection* circuit is set. The scan result is then delivered to the S lead in the bit 7 position of time slot 22.

Table I lists the digital signals that are sent from or received by the remote line concentrator. The implementation of the multifunctional circuits described above will be discussed in the following sections.

IV. TIMING CIRCUIT

The timing circuit performs the following functions:

i. recovers the basic 1.536-mc timing signal from the C lead addresses;

ii. counts this signal down by eight to generate bit pulses at 192 kc, thus defining the time slots;

iii. frames the eight's counter by detecting a unique signal consisting of eight consecutive ones sent out on the R lead in the last time slot;

iv. combines and amplifies the above signals and distributes them to various parts of the remote line concentrator.

The diagram of the timing circuit is shown in Fig. 3. A slave clock extracts the basic 1.536-mc timing signal by passing the C lead bits through a quartz crystal filter. To insure adequate timing signals during low-traffic periods, pulses on the C lead represent "zeros" instead of "ones". The output signals are amplified and two phase pulses, ϕ_0 and

TABLE I—DIGITAL SIGNALS WHICH ENTER OR LEAVE THE REMOTE LINE CONCENTRATOR

From or to	Name of signal	Sent via (see Fig. 2)	Time when sent or received by controller	Purpose
A. To concentrator	1. Line gate number (LGN)	C lead	Bits 0 through 7 of time slots 0 through 22 in every frame	Orders operation of line gate, thereby sampling
	2. Scan gate number (SGN)	C lead	Bits 0 through 7 of time slot 23 in frame 0	Scans idle lines to determine whether they are "off-hook"*
	3. PCM speech or tone	R lead	Bits 0 through 6 of time slots 0 through 22 in every frame	Delivers speech or tone signal to decoder
	4. Scan command	R lead	Bit 7 of time slots 0 through 22 in frame 0	Adds scan order to signal A1*
	5. Framing command	R lead	Bits 0 through 7 of time slot 23 in every frame	Orders reset of counters in slave clock
B. From concentrator	1. PCM speech	S lead	Bits 0 through 6 of time slots 0 through 22 in every frame	Transmits speech signal from encoder
	2. Scan result	S lead	Bit 7 of time slot 22 in frame 1 or 2	Indicates if line scanned (A2 or A4) was "off-hook"

* Either A2 or A4 is used (not both)

ϕ_2, are generated by blocking oscillators. The ϕ_2 pulse advances an eight-stage re-entrant shift register which generates the bit pulses. The framing signal from the eight-ones detector insures that this counter has a single one circulating in the correct phase.

The framing signal is generated by the eight-ones detector, another eight-stage shift register. Whenever a one appears on the R lead, a one is advanced into the register. The arrival of a zero resets the register to zero. A consecutive string of eight ones will advance a one into the eighth stage, and its output is "ANDed" with the last input one, delayed by one-half microsecond, to give the "frame" signal. This signal resets the first seven stages to zero. The last stage is reset when the next one arrives on the R lead; this reset operation is designed to avoid a race condition.

The frame signal sets the inhibit flip-flop, which in turn inhibits the send and receive gates in the framing time slot. This is done to prevent sampling in time slot 23, which would introduce annoying ticks in the telephone being scanned.

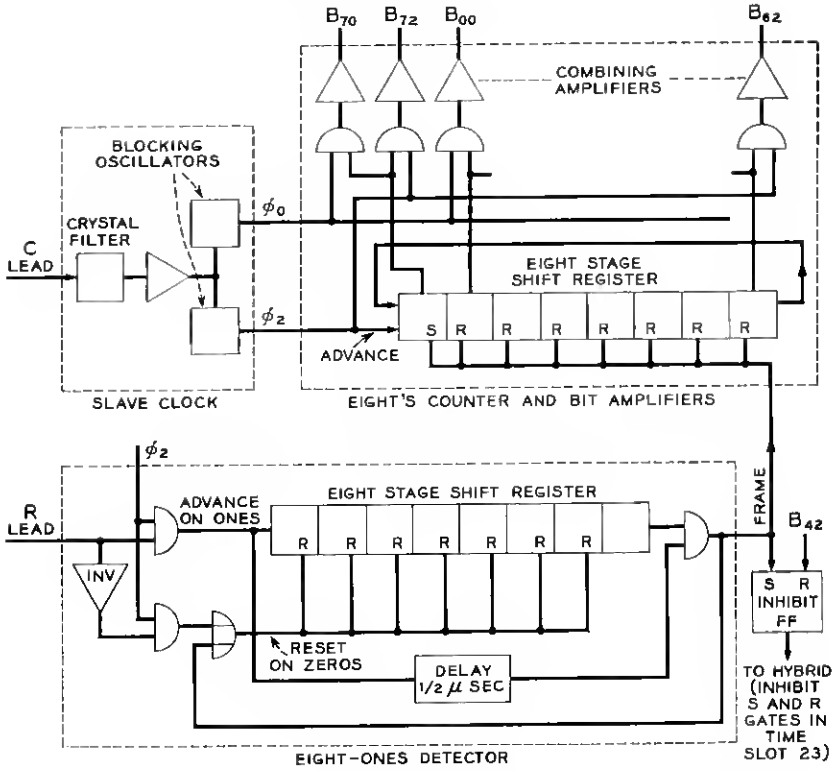

Fig. 3 — Timing circuit.

The eight outputs from the eight's counter are combined with the phase pulses, ϕ_0 and ϕ_2, and amplified to form all the other timing signals required by the remote line concentrator.

V. SELECTOR

Eight-bit addresses carried by the c lead are delivered to the selector (Fig. 4). The serial eight-bit words are advanced through a shift register and, when they have stepped completely into the register, are read out in parallel through AND circuits. Both the bits and their primes are stretched in time to 2 microseconds and amplified by 16 stretching amplifiers. The first four bits and their primes become the inputs to a 1-out-of-16 diode matrix consisting of 16 four-input AND circuits selecting one out of 16 output leads. The second four bits and their primes select one out of 16 output leads of a second diode matrix. The two active leads

from the diode matrices enable two flip-flops, one each in two banks of 16. The setting of the flip-flops is timed by an enabling clock pulse labeled "set". This pulse occurs one microsecond later than the "read" pulse, which interrogated the shift register. The outputs of the flip-flops are transformer-coupled into transistor amplifiers. The collectors of one set of 16 amplifiers in the common emitter configuration provide the verticals of a 16-by-16 coincident-voltage matrix. The emitters of the other set, in the common collector configuration, provide the horizontals of this matrix.

The primaries of the subscriber line gate pulse transformers are connected between the horizontals and verticals of this 256-point matrix.

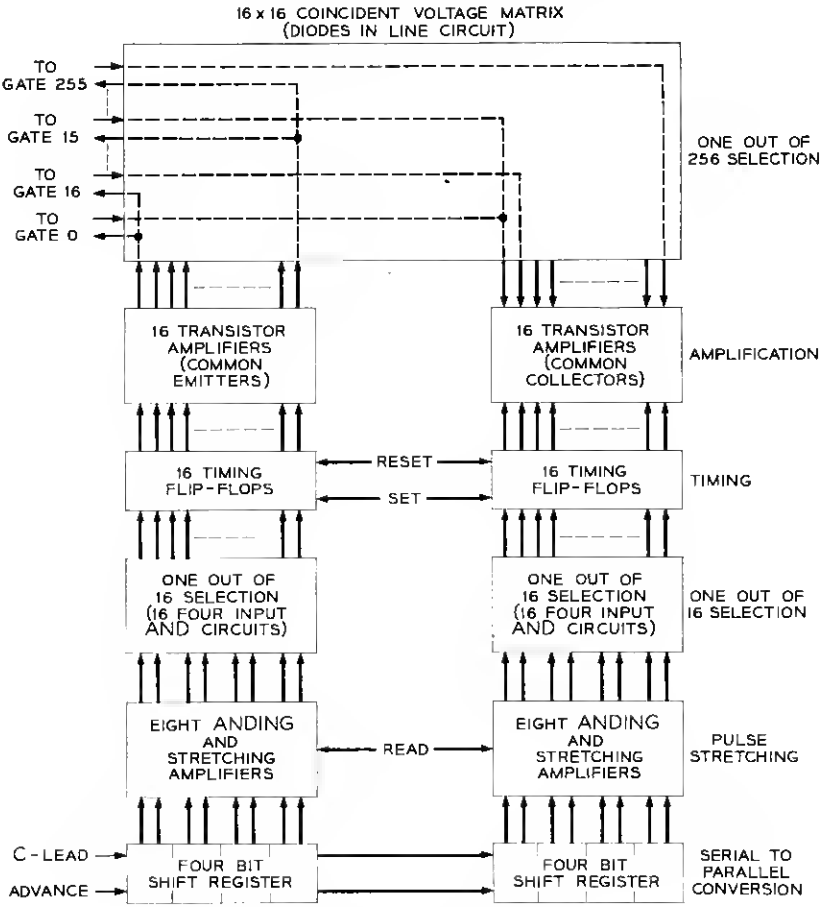

Fig. 4 — 1-out-of-256 selector.

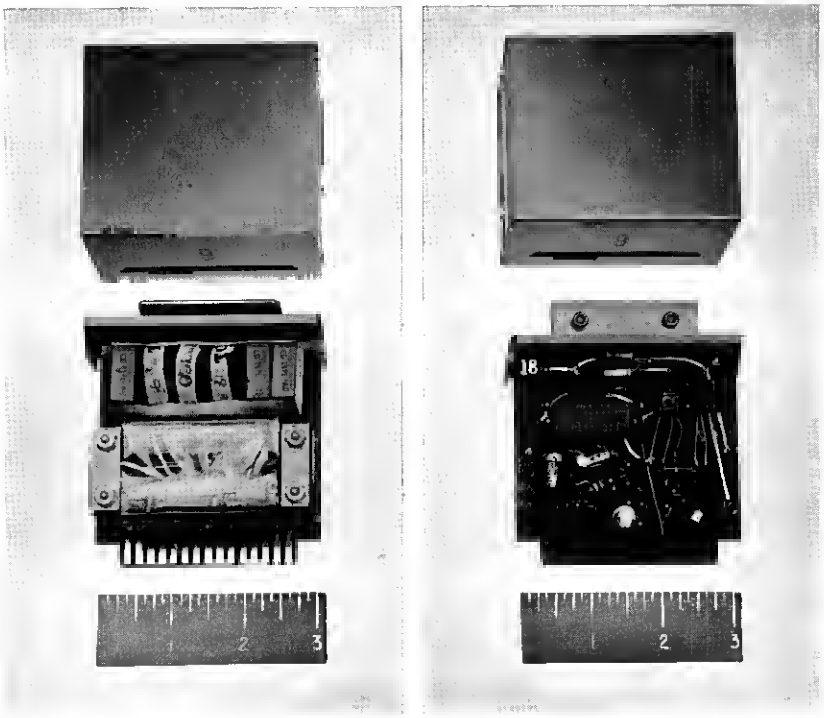

Fig. 5 — Subscriber line circuit package.

A diode to prevent "sneak" paths is located in series with the primary of the pulse transformer in the line circuit module.

The common collectors are connected to −6 volts and the common emitters to ground. When a vertical and a horizontal are selected, the 6 volts applied across two ON transistors, one diode and the primary of the gate transformer allows 80 milliamperes of current to flow in the primary of the transformer. Three microseconds later, the timing flip-flops are reset, interrupting the current flow.

Small signals resulting from parasitic capacities appear on the inputs to unselected gates that share either verticals or horizontals with the selected gate. These unwanted signals are caused by the discharging of wiring capacities through the primary windings of the unselected gates. They can be reduced below the threshold of the gate by adding a resistor (10,000 ohms) from each horizontal and each vertical to a point at −3 volts. Thus, all wiring capacities are charged to the same voltage and all unwanted signals become equal and less than those needed to cause a gate to conduct.

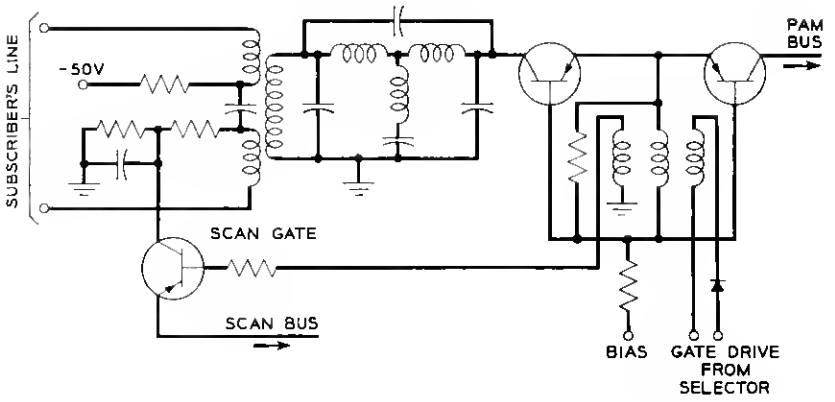

Fig. 6 — Subscriber line circuit diagram.

VI. SUBSCRIBER LINE CIRCUIT

The two-wire subscriber line circuit, one of which is provided for each line, is arranged so that it can be installed as required. It is the smallest module in the system, but one of the most important, since it has such a large effect on the per-line cost of the system. A photograph of the subscriber line circuit package is shown in Fig. 5.

The subscriber line circuit contains a time-division gate, a low-pass filter, a scan gate and a repeat coil. The repeat coil is used to match the 900-ohm telephone to the 2000-ohm filter, and to isolate the time-division gate from the common battery required by the telephone. A circuit diagram of the subscriber line circuit is shown in Fig. 6.

The time-division gate[3] consists of two nearly symmetrical alloy germanium transistors. These are connected emitter to emitter and base to base, with a pulse transformer winding connected between base and emitter. The application of a 80-milliampere current pulse will enable the gate to pass a peak signal current of about 400 milliamperes from collector to collector. In this state, the gate looks like a 2-ohm resistor. When the current pulse is removed, tbe gate returns to its high impedance state. In the experimental system, which uses 2N417-type transistors, about 2 microseconds is allowed for this purpose, providing the desired adjacent channel crosstalk level of 75 db. In the absence of a pulse, the gate is a bigh impedance. To increase the isolation obtained in the off condition, a bias voltage is applied to the gate through a resistor, insuring that the collectors are back-biased during the maximum positive swing of the voltage on the filter or on the PAM bus. The resistor also helps to reduce crosstalk produced by the junction capacity of the transistors.

The time-division gate limits the maximum rms sine-wave power-handling capacity of the system. The desired crosstalk level fixes the time that must be allowed for turn-off of the gate, and thus determines the "on" time of the gate, since the time slot width is fixed. The drive available from the selector sets the maximum current the gate can pass. The breakdown voltage of the transistors in the gate, minus the bias voltage, determines the maximum signal voltage swing allowed. Since the maximum voltage swing and peak current are limited by the gate transistors, the power-handling capacity of the gate and the operating impedance level of the filter are specified.

Time-separation systems require a low-pass filter to isolate the subscriber's line from the frequencies generated by the operation of the sampling gate.[4,5] In addition to having good out-of-band rejection, the filter should also have fairly constant impedance characteristics within the pass band. However, since a filter per line is required, it is desirable, from an economic standpoint, to use as few components as possible. These somewhat conflicting filter requirements generally lead to a compromise design. The low-pass filter in the experimental unit is a two-section insertion loss design having a characteristic impedance of 2000 ohms. The impedance level was determined by the factors discussed in the preceding paragraph.

The line scanning procedure was described in Section III. The subscriber line circuit is provided with a scan gate that delivers a pulse when the line circuit is pulsed by the selector and the telephone is "off-hook" and drawing current. The resulting pulse is delivered to the scan bus. If the line is being scanned, the scan command that appears at bit 7 time on the R lead and the pulse on the scan bus will set the scan flip-flop storing the scan result. This result is delivered at the proper time, through the scan result injection circuit (Section X), to the S lead.

The design of the line circuit is influenced to some extent by the type of telephone used. The laboratory models of the subscriber line circuits were designed to work with a transistorized telephone requiring about two-thirds of a watt. This power is obtained from a 50-volt common battery through current-limiting resistors located in the line circuit. The telephone is equipped with a tone ringer, which gives substantially the same acoustic power output for tone voltages that vary from 0.5 to 2 volts.[6] These ringing levels fall well within the power-handling capacity of the subscriber gate. A slightly modified line circuit will allow conventional telephones with electromechanical ringers to be used.

VII. TIME-SHARED HYBRID

Signals from subscribers' telephones are carried to the remote line concentrator by balanced two-wire cables. Signals are carried between the remote line concentrator and its concentrator controller on a four-wire system. A hybrid thus is needed to convert between the two-wire and four-wire systems.

Two alternative arrangements were considered: (a) a voice-frequency hybrid and (b) a time-shared hybrid. A voice-frequency hybrid arrangement requires for each subscriber's line a sending gate and filter, a receiving gate and filter and a voice-frequency hybrid. A time-shared hybrid arrangement requires one filter, one gate and a repeat coil for each subscriber's line plus a share of a common hybrid. The second arrangement was used. The selected line gates connect all active subscribers' circuits via a common two-wire PAM bus to the time-shared hybrid (Fig. 7).

The hybrid consists essentially of a send gate and a receive gate, which are identical to the subscriber gates. Since send signals must be stretched

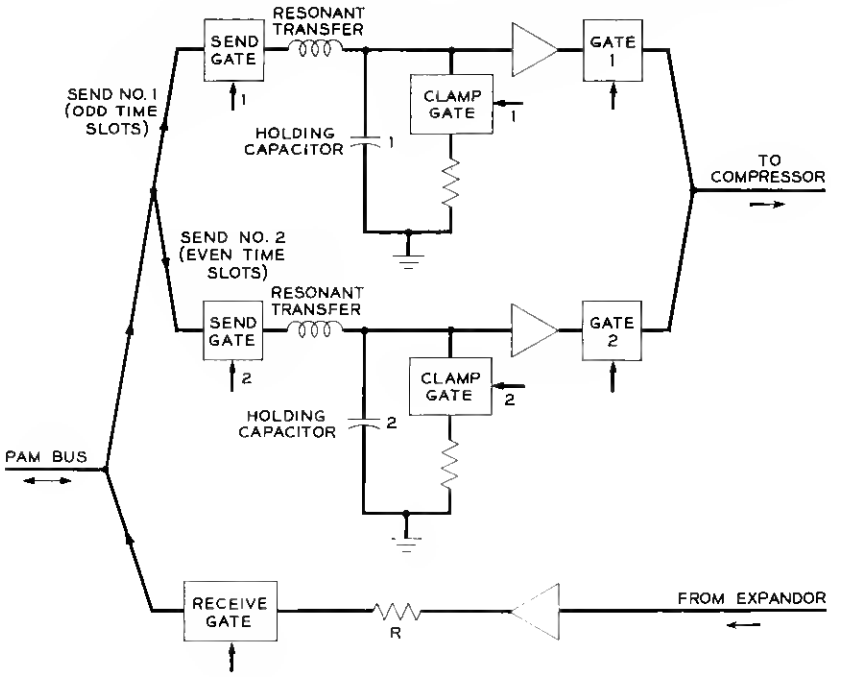

Fig. 7 — Time-shared hybrid.

for nearly one time slot for the coding operation, two send gates are operated in alternate time slots under the control of a binary counter. The hybrid works in the following fashion: the send gate is operated at the same time as the line gate and remains in operation for one microsecond; it then opens up and, after 0.3 microsecond guard space, the receive gate operates, opening 1.6 microseconds later with the line gate (Fig. 8). A received PCM signal is decoded and amplified, goes through the receive gate to the PAM bus, then goes through the line gate and

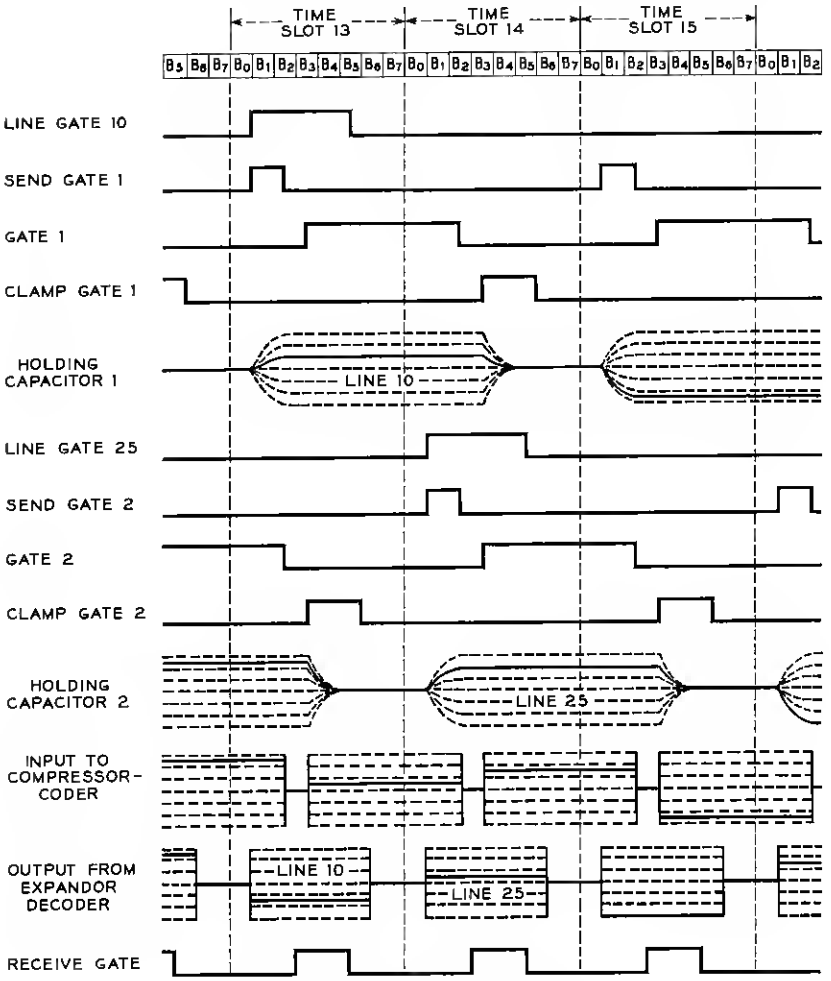

Fig. 8 — Timing of the time-shared hybrid.

charges the shunt filter capacitor. The line gate then opens. During the subsequent 122 microseconds this signal is dissipated in the subscriber's telephone so that very little remains to be sampled when the line gate and the send gate again operate together.

If the subscriber's filter is not matched correctly by the subscriber's telephone, the signal will be reflected and sampled by the send circuits. Thus, the time-division hybrid has properties similar to conventional hybrids except that it is lossless.

The actual circuit (Fig. 7) shows that resonant transfer of charge from the filter capacitor to a pulse-stretching or holding capacitor is used. The stored signal is then amplified and switched through another gate to the compressor. The amplifier has a high input impedance and is used to prevent discharge of the holding capacitor. When the coding action is completed, the stored energy is clamped out with another gate. While PAM signals are being coded in an odd time slot, the second send circuit is sampling in an even time slot.

In the receiving portion of the hybrid, the output of decoder and expandor is amplified by a common amplifier and passes through the receive gate, PAM bus and line gate, and charges the shunt filter capacitor of the line circuit to the value detected by the send sampling in the other concentrator. Resonant transfer is not used in the receive circuit, since any residual signal in the line package should be dissipated, thus terminating it. If the residual signal is dissipated, then the four-wire loop can have unity gain with misterminated line circuits and still not sing. This has been verified both mathematically and experimentally.[7]

Fig. 9 shows the hybrid timing circuits that control the operation of the seven gates in the hybrid. Each gate is driven by a flip-flop controlled transistor amplifier and each amplifier produces a 100-millampere pulse. Another flip-flop, connected as a binary counter, causes the two send circuits to operate in alternate time slots. An inhibiting signal from the inhibit flip-flop located in the timing circuits (Section IV, Fig. 3) prevents the send and receive gates from operating in time slot 23 when scanning takes place.

VIII. COMPRESSOR AND EXPANDOR

The send PAM signals are switched into a shunt compressor, which has a nonlinear resistance characteristic obtained by the use of carefully matched, temperature-controlled diodes. The network is designed so that the loss is increased with increasing signal amplitude. Large signals are attenuated by 26 db relative to small signals. This characteristic, to-

gether with linear encoding, has the effect of spreading small signals over a greater number of levels, thus reducing the quantizing noise.[8] In the receive circuits an expandor uses a similar, but series, network to obtain the inverse characteristic.

The actual circuits are shown in Fig. 10. The compressing network is followed by a high-input-impedance feedback amplifier, which provides sufficient signal for the encoder. The expandor network has both a preamplifier and a postamplifier. The preamplifier, which has a constant-voltage output characteristic, drives the series network, and the resulting current is amplified by a low-input-impedance postamplifier. The postamplifier is followed by the common medium-power amplifier in the hybrid, which charges the line circuit shunt filter capacitor.

IX. ENCODING AND DECODING

The output of the compressor is fed into a 128-level feedback-type encoder[9] (Fig. 11), which, in essence, consists of a summing amplifier

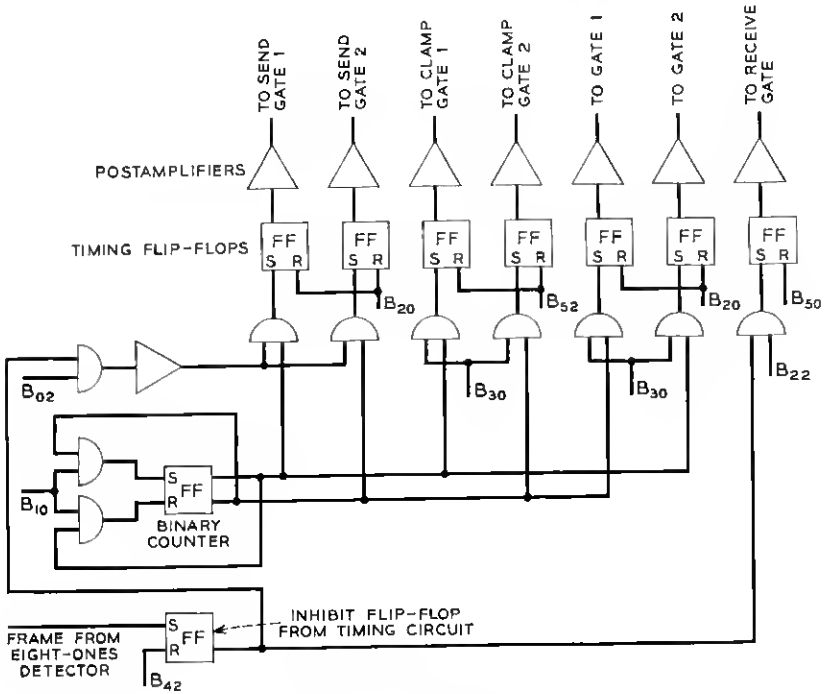

Fig. 9 — Hybrid timing circuits.

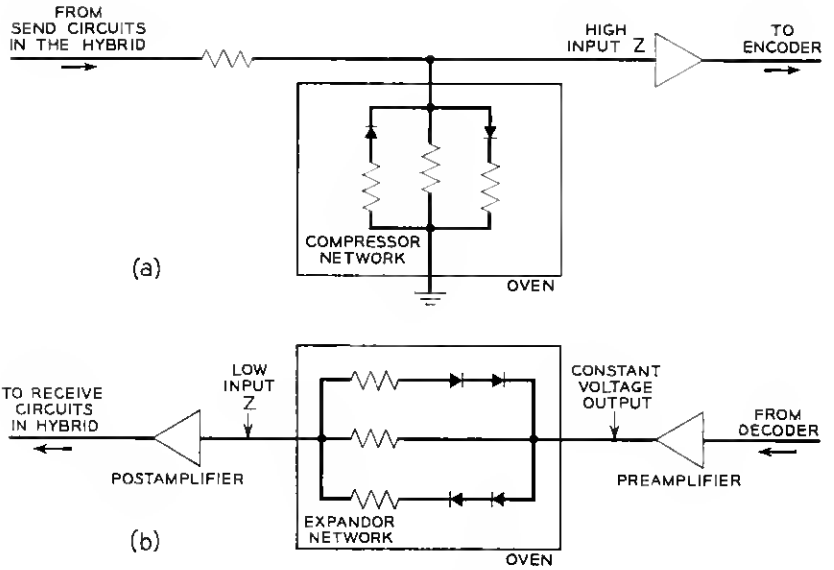

Fig. 10 — Compressor and expandor.

and a programmed decoder. Seven binary weighted resistors, of values R, $2R$, to $64R$, can be connected to either ground or a negative reference voltage according to the state of seven memory elements. The memory elements consist of blocking oscillators so connected that, when triggered, they will give out a series of pulses 0.3 microsecond wide every 0.65m icro-

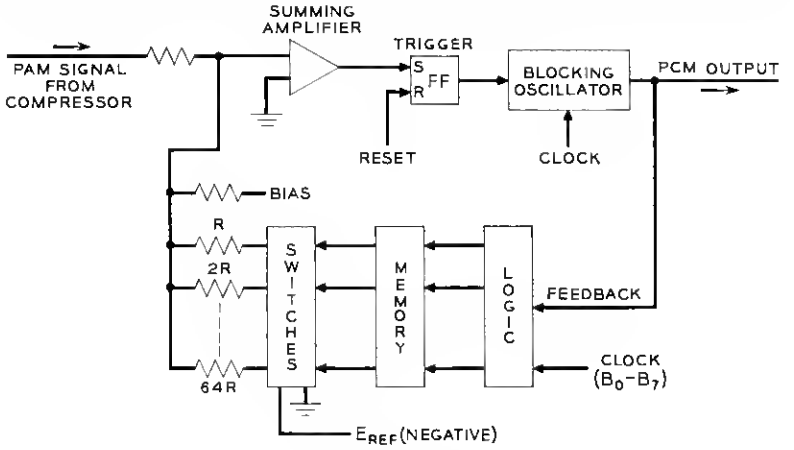

Fig. 11 — Encoder.

seconds. The blocking oscillators can be stopped if an inhibiting signal is applied immediately after the first pulse.

The PAM signal from the compressor is fed into a summing amplifier. A fixed bias raises this signal so that a zero-level input signal will be encoded as level 64 and a maximum amplitude negative signal as level zero. A third input comes from the binary weighted network, whose resistors are successively connected to either a negative reference voltage or ground until the total contribution from the three sources, i.e., signal, bias and network, is zero. Fig. 12 illustrates the encoding of a PAM signal corresponding to level 91.

During the first bit time of the coding interval, the resistor of value R is connected to ground, all other resistors being connected to the negative reference voltage. If the resultant signal to the summing amplifier is positive, then the trigger circuit and output blocking oscillator fire, sending out the most significant PCM bit. A feedback signal to the logic and then to the memory element causes the most significant bit resistor to be reset; i.e., it will be connected to negative for each successive trial. If the resultant signal to the summing amplifier is negative, then a zero would be sent out for the PCM bit and the feedback would cause the

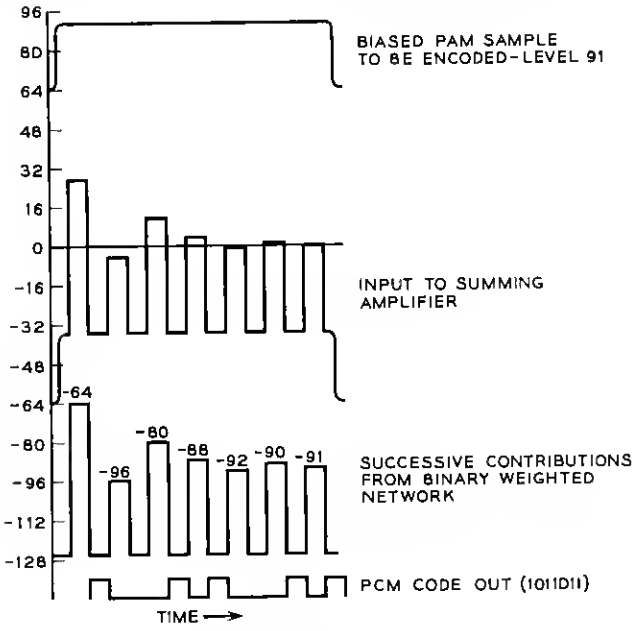

Fig. 12 — Waveforms in the encoder.

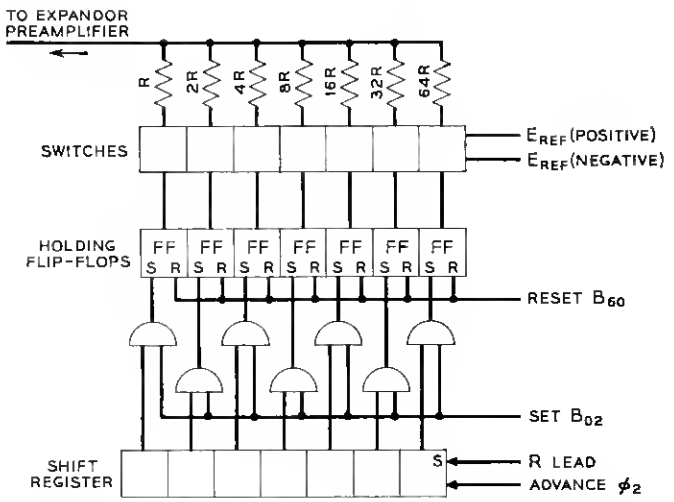

Fig. 13 — Decoder.

contribution from the most significant resistor to remain. In the successive bit periods, resistors of value $2R$, $4R$, through $64R$ are tried until the final code is reached and the resultant signal to the summing amplifier is zero.

The decoder is shown in Fig. 13. It consists of a shift register that converts incoming PCM code on the R lead from serial to parallel. When the code has completely stepped into the register, the bits are read out in parallel into holding flip-flops, which, in turn, operate transistor switches. The switches connect binary weighted resistors R, $2R$, through $64R$ to either negative or positive reference voltage according to the state of the holding flip-flops. The resultant decoded signal is then amplified by the expandor preamplifier, expanded and delivered to the hybrid. The holding flip-flops in the decoder are reset after a $5\frac{1}{2}$-bit time interval.

X. SCAN RESULT INJECTION

The s lead carries two types of signal; seven bits of PCM-coded speech in time slots 0 through 22 and the scan result in the bit 7 position of time slot 22 (Table I). The scan result is generated on the scan bus as soon as the line gate is operated. If a line is to be scanned, there will be a bit in the bit 7 position on the R lead. If this number corresponds to an active line, the bit is in the assigned time slot. If the number is inactive, both the address and the scan command, part of the framing signal, are in the last time slot. In either event, the result of scanning is gated to the "set" input of the scan flip-flop, Fig. 14, which stores the information until the bit

7 position of time slot 22 of the s lead words. At this time, the state of the scan flip-flop is interrogated and sent out over the s lead. The scan flip-flop is reset a few bits later under the control of the inhibit flip-flop signal. The two signals, seven-bit PCM plus the scan result, are amplified and pulse shaped, and drive the s lead cable pair.

In addition to scan result injection, one can add other signals in time slot 23 that would monitor the state of the remote line concentrator.

XI. LABORATORY MODEL

The laboratory model of the remote line concentrator, shown in Fig. 15, is contained in two 39-inch cabinets. The left-hand cabinet contains the subscriber line circuits and the 1-out-of-256 selector; the right-hand cabinet contains the remainder of the equipment. The division of the experimental model of the remote line concentrator into two parts was a result of the way in which the experiment was implemented. This implementation was divided into three parts, called Phases 1, 2 and 3.

In Phase 1, two cabinets were made, each of which contained subscriber line circuits, time-shared hybrids and selectors. The units were tested by connecting them with coaxial cables that carried the PAM signals. In Phase 2, the encoders, decoders, expandors, compressors, timing circuits, delay lines and a primitive form of central stage switch were added. Additions were made on a circuit-by-circuit basis — checking, testing and consolidating before moving on. The work on the remote line concentrator was essentially completed at the end of Phase 2. Phase 3 consisted of adding the concentrator controller, central stage switch and common control simulator.

This procedure permitted circuits and features to be added to the unit as required. The completed portion of the concentrator was therefore kept on a solid basis, which enabled it to be used as the test facility for

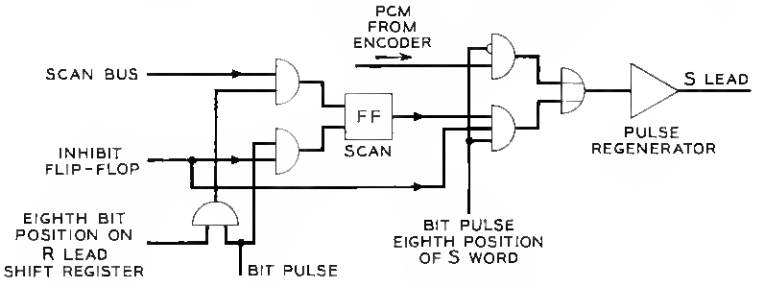

Fig. 14 — Scan result injection circuit.

Fig. 15 — Remote line concentrator.

new circuitry and eliminated the need for synthesizing environmental conditions. One of the most attractive features of this procedure was the elimination of that most trying period that occurs when individually constructed circuits or groups of circuits are completed and then assembled and welded, hopefully, into a complete unit.

The laboratory model contains all the circuits and features required by the system, except for the number of subscriber line circuits installed. Twelve subscriber line circuits are installed in each remote line concen-

trator. Provision was made so that these could be connected to any number point on the 1-out-of-256 selector by means of a plugboard mounted in the back of the cabinet (Fig. 16).

The problems of equipment design were considered an integral part of the ESSEX experiment. Rigid standardization of layout and wiring was not employed, since it was recognized that new ideas and techniques would occur and become available during the course of the experiment. When any new ideas or techniques were proven satisfactory they were incorporated in the later units, no attempt being made to change or rework any of the finished units. The rear view, Fig. 16, of the remote line concentrator at an early stage of the experiment is an excellent example of this. The rack, on the right, which contains the subscriber

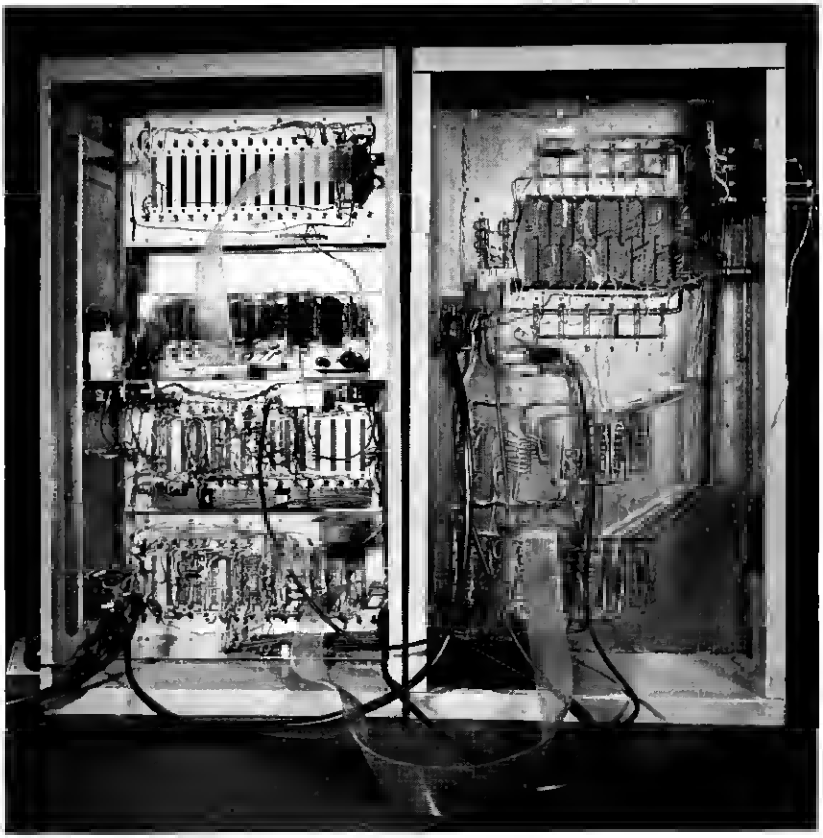

Fig. 16 — Rear view of remote line concentrator.

line equipment and the 1-out-of-256 selector was the first unit made. This single-panel construction was found to be inflexible, and the subpanel arrangement shown in the left-hand rack, in Fig. 16, was adopted. This arrangement was used in the concentrator controllers, the trunkor unit, the trunkor controller, the central stage switch and the common control simulator.

Each subpanel can accomodate 15 printed circuit cards, which plug into printed circuit connectors. Interconnections between printed circuit connectors on the same subpanel were made with color-coded plastic-covered stranded wire, no particular attempt being made to keep these interconnections as short as possible. Power and clock pulses were brought into the subpanels by means of printed circuit cards, which plugged into multiples located in troughs on the left and right walls of the cabinet. Interconnections between subpanels and between cabinets were made with flat multiconductor cable. Several types of cable were used in order to determine the advantages and disadvantages of each.

The individual circuits are mounted on 5- by 8-inch gold-plated printed circuit cards. Most of the analog circuits and some special purpose digital circuits, such as the encoder and 1-out-of-16 selector, are located on cards laid out for the specific circuit or groups of circuits involved. Special-purpose cards were not used for the digital circuits. Instead, three cards were provided, one containing five flip-flops, another holding eight pulse amplifiers and the third being laid out to accomodate AND and OR logic circuits and emitter followers. The digital circuits were formed by cross-connections on the printed circuit connectors on the rear of the panel. To make this scheme work effectively, each part of a digital circuit was given a number that located the card and the position location of the circuit on the card. Examples of typical printed circuit cards are given in Fig. 17. The card in the upper left-hand corner contains eight pulse amplifiers, the card in the upper right-hand corner contains the 1-out-of-16 selector. The lower card contains five flip-flops. Wherever possible, the circuit diagram, input and output connections and supply voltage busses have been clearly marked. This relatively minor detail has been a great aid and time saver in fault location.

The logic circuits used were mostly AND and OR circuits in conjunction with flip-flops and amplifiers. These circuits used the fastest transistors and diodes commercially available at the start of the experiment. Even so, in order to obtain the 50-millimicrosecond rise and fall times required, clipping and clamping techniques had to be used. This can be seen in Fig. 18, which shows the circuit diagrams of the pulse amplifier and flip-flop used in the experimental system.

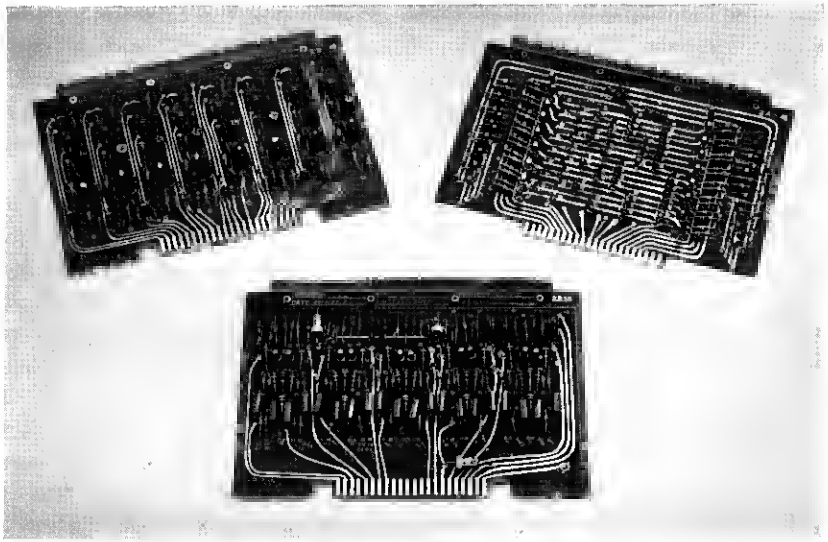

Fig. 17 — Printed circuit cards.

The power required by the remote line concentrator, exclusive of telephones, is 75 watts. The transistorized telephones used in the experiment required two-thirds of a watt each. Methods of powering the remote line concentrator have been considered, but not in any great detail. Power for the experimental system was obtained from a bank of commercially available transistor-regulated supplies.

The measured terminal-to-terminal transmission characteristic of the system is 6 ± 0.5 db from 100 to 3200 cps, and the 9-db points are at 70 and 3500 cps, with very small variability from channel to channel. The midband loss of the system was set at 6 db for convenience, and does not represent the minimum loss obtainable in a stable system. The minimum loss obtainable is twice the loss in a subscriber line circuit.

The seven-bit PCM with logarithmic compression gives a signal-to-noise ratio of about 30 db for a large dynamic range of signals. A simple demonstration of the noise introduced into the system by the PCM encoding and decoding has been incorporated into the experiment. This is done by operating a key, which drops out the PCM and connects the terminals of the filters on one channel by means of a physical pair. The difference is observable only in a very quiet room. Usually, however, the quantizing noise is almost completely masked by room noise.

The measured crosstalk level is 65 db down from an adjacent channel in the same remote concentrator. As explained earlier, the analog cir-

cuits and the high-level pulses present at the output of the 1-out-of-256 selector must be laid out very carefully in order to achieve this result.

At the time this paper was written, the remote line concentrator had been operating for a period of ten months. During the last two months it was operated over a 25-mile microwave link between Murray Hill and Holmdel, New Jersey. Since only one microwave channel was available from Murray Hill to Holmdel, the R and C leads were multiplexed onto the channel at Murray Hill and demultiplexed at Holmdel.

An artist's sketch of what an ESSEX remote line concentrator might look like when condensed into a single unit is shown in Fig. 19. In this conception, the subscriber line equipment is installed in the doors, with 128 subscriber line circuits in each door. Traffic consideration in an operating system would require that about 115 subscribers be connected to a remote line concentrator. In this case, one door could be replaced by a cover plate. The central portion contains all the shared circuits of

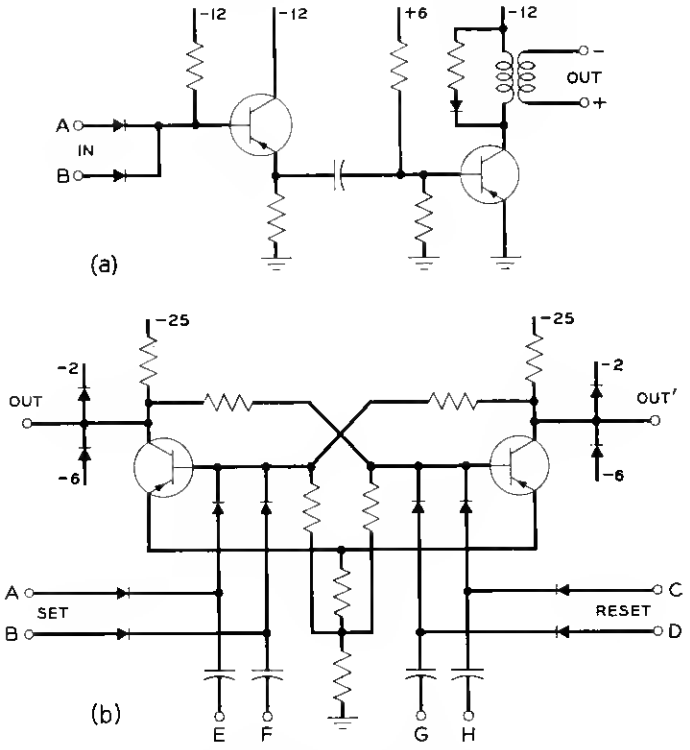

Fig. 18 — Pulse amplifier and flip-flop circuit diagrams.

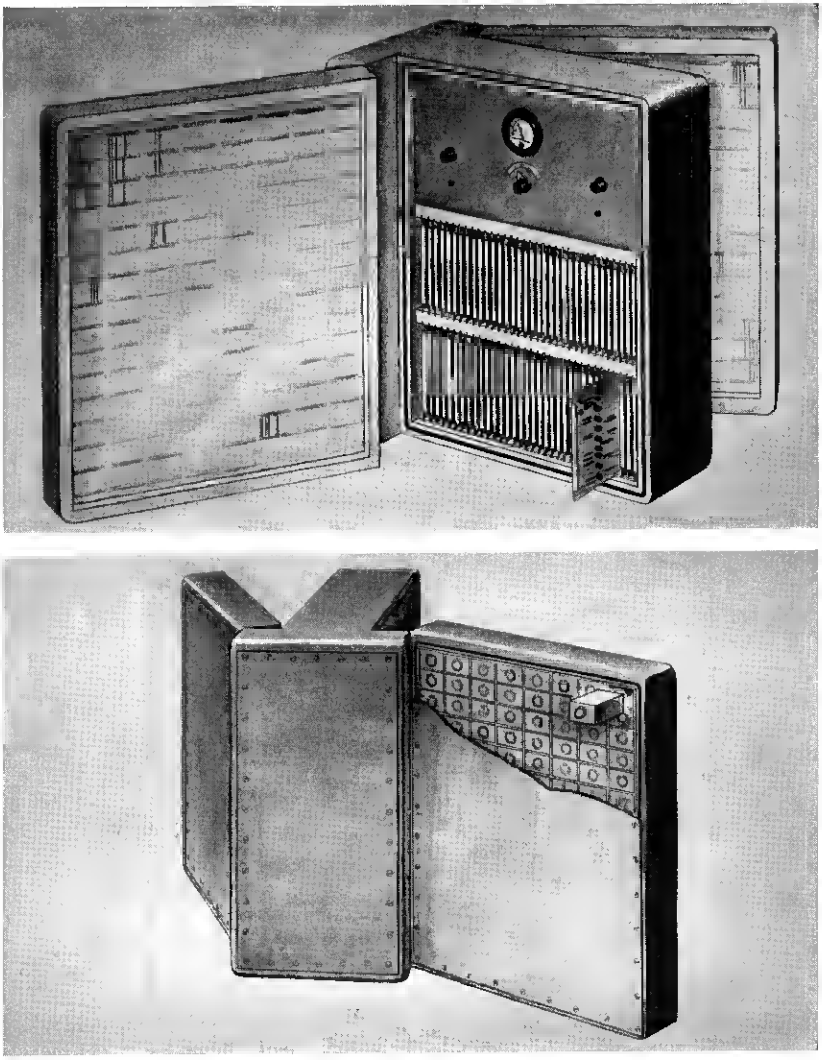

Fig. 19 — Artist's conception of remote line concentrator.

the unit and space for a remote power supply and four-hour battery standby if required. The unit, as pictured, would measure 16 × 27 × 30 inches with both doors closed, and would weigh approximately 250 pounds. The size and weight figures were obtained from the equipment used in the experimental version of the remote line concentrator.

XII. SUMMARY

Two remote line concentrators and a trunkor have been built and have operated successfully in the experimental environment. The units work at the required speeds. The design is straightforward. The implementation presented few problems of any magnitude and required no change in the basic system plan. This, in very large measure, is a result of the fundamental simplicity of time-division switching and digital communication systems.

XIII. ACKNOWLEDGMENTS

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